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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,533	02/27/2002	Eric DeLano	10016665-1	7692

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,533	DELANO, ERIC	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 3-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

STATUS OF CLAIMS

1. Claims 1, 3-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5692121 to Bozso et al.

2. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5692121 to Bozso et al. as applied to claim 12 above, and further in view of US 5568380 to Brodnax et al.

3. Claim 2 is cancelled.

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1, 3-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5692121 to Bozso et al.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5692121 to Bozso et al. as applied to claim 12 above, and further in view of US 5568380 to Brodnax et al.

Response to Arguments

8. Applicant's arguments filed 5 November 2004 have been fully considered but they are not persuasive. Regarding Applicant's argument (page 7) that "checkpointing

refers an 'end' of a time period... In Bozso, "checkpointing occurs on a per-instruction basis."...", further referring to the "architectural" state of the processor, Examiner notes that Applicant has only claimed "storing... prior to architecting" and "periodically checking for data errors". Applicant has claimed actions relative to each other, not relative to an absolute reference, e.g. a clock. While "periodically" may imply the use of such an absolute, it merely implies that it occurs on a some regular or predictable interval, which Bozso et al.'s "per-instruction" basis achieves. Examiner notes that Bozso et al.'s instructions are further executed on a cyclical basis (see, for example, figure 2A).

9. Regarding Applicant's argument (page 7) that Bozso et al. does not store a copy of a register of a register file within a buffer prior to writing new data to the register, Examiner points to the pipeline type structure illustrated in figure 2A and B wherein instructions are executed in sequence. Element 41a is used to store the processor's "current state", i.e., a register file. Data from this register file is then transferred to a checkpointed state, i.e. Applicant's claimed "buffer", in the subsequent cycle, element 51a. Examiner further notes that sequential instruction execution, e.g. the pipelined processor of Bozso et al., operates by moving an instruction through each cycle (as illustrated in Bozso et al.), one after the other. Examiner further notes from line 60 of column 8, "Note that Cycle 3 (during which a transfer takes place from a Current State array to the Checkpoint array), corresponding to the completion of an instruction, can be concurrent with a Cycle 2 of the subsequent instruction. In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully

completed state change is transferred form the Current State array to the Checkpointed State array."

10. Regarding Applicant's argument (page 8) that claim 3 requires that new data is written to the register after a copy of data in the register is stored within the buffer, Examiner again notes from line 60 of column 8, "Note that Cycle 3 (during which a transfer takes place from a Current State array to the Checkpoint array), corresponding to the completion of an instruction, can be concurrent with a Cycle 2 of the subsequent instruction. In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array." Wherein Cycle 3 and Cycle 2 are one cycle apart, hence "Cycle 3" and "Cycle 2".

11. Regarding Applicant's argument (page 8) that claim 4 requires "new data is loaded to the register concurrently with the step of [sic] loading [storing]", Examiner again notes from line 60 of column 8, "Note that Cycle 3 (during which a transfer takes place from a Current State array to the Checkpoint array), corresponding to the completion of an instruction, can be concurrent with a Cycle 2 of the subsequent instruction. In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array." Wherein Bozso et al. have explicitly stated that Cycle transfer from Currrent State to Checkpoint can occur "on the same cycle" as a "newly arriving state can be written into the Current State array".

12. Regarding Applicant's argument (page 8) that claim 6 requires that the buffer is flushed after checking for, and detecting no, errors, Examiner cites Applicant's own specification from paragraph 22 of the pre-grant publication, "If no errors exist, the buffer is flushed, at step 112, so that new data may be stored within the buffer and for a period extending to the next checkpoint; processing thereafter proceeds at step 102, as shown." Examiner cites from line 39 of column 8 of Bozso et al., "Following ENDOP, and following a successful comparison of results from the two processors, each result is checkpointed by the R-Unit. At that point, the aggregate Current State array 41a, 41b is transferred to the Checkpointed State array 51a, 51b in a final cycle if the ES flip-flop 37 indicates that no errors have occurred. Each checkpointed result is protected by ECCs so that soft errors in the checkpointed state can be corrected." Clearly, in this pipelined processor, data that passes the ECC check gets pushed to the Checkpointed State array, pushing the previous contents out, or "flushing" the array.

13. Referring to Applicant's argument (page 8) that Bozso et al. does not disclose re-executing a program nor resetting a program counter, Examiner reiterates, from line 47 of column 8, "If there is a miscompare prior to checkpointing, then the checkpointing operation is inhibited, and the processor state is recoverable to the point that is consistent with the last successful checkpoint operation. Recovery is performed by small state-machines in the I-Unit and E-Unit. The I-Unit state-machine reads all 128 registers in sequence. As each register is read, the R-Unit corrects any latent soft errors. The E-Unit state-machine updates all shadow copies of these registers (i.e., the actual working registers) from the checkpointed state, and it rewrites the checkpointed

state back into the R-Unit. This completely "scrubs" the processor state, and recovers the processor to the point of the last successfully completed operation." Wherein the processor starts processing the instruction stream again from the checkpoint, arriving at a prior point in the current state of processing.

The system of Bozso et al. operates by executing instructions, such instructions are executed cyclically in a pipeline. On error, the processor is reverted to a known good state and processing continues from that point. Examiner has provided a prima facie case to Applicant, however, Applicant has responded by merely alleging that the proposed elements are not present. In order to overcome this rejection, Applicant must show how Bozso et al. does not, in fact, operate identically to Applicant's claimed invention or, alternatively, amend.

14. Regarding Applicant's argument (page 8) that the "formal checkpointing or storing... on a per-instruction basis" of Bozso et al. does not disclose "periodically checking for data errors at sequential time periods defined by a number of processing cycles", see paragraph 8 above. Further, Examiner notes that the instructions of Bozso et al. are executed cyclically, as are the ECC and checkpointing processes. Clearly, if there is a difference between Bozso et al. and the Applicant's invention, claim 10 does not sufficiently claim this difference.

15. Regarding Applicant's argument (page 9) that Bozso et al. does not disclose a plurality of pipelines for processing program instructions relative to a program counter, see figure 2A and B wherein instructions are split, cyclically.

Further, regarding "pipeline stages loading data into a register of a register file", see figure 2A and B, elements 41A and B.

16. Regarding Applicant's argument (page 9) that Bozso et al. does not disclose "an additional read port [sic] from [for] reading data from the register". From line 63 of column 8, "In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array. In short, any location in the Current State array can be read-from and written-to in the same cycle, and the array is constructed to allow this without corrupting the output data with the input data." Further, see figure 2A and B, wherein the write enables of both processor A and B read from 41A in addition to 51A.

17. Regarding Applicant's argument (page 9) that Bozso et al. does not disclose a program counter being reset in connection with the buffer restoring data to the register file, see paragraph 13 above.

18. Regarding Applicant's argument (page 10) that neither Bozso et al. nor Brodnax et al. teach reading data from a register prior to writing to that register, Applicant has not claimed the immediacy of sequence or the contiguousness of instructions. For example, in figure 4 of Brodnax et al., clearly, two instructions (3 and 8) are executed involving checkpointing. In this example, instruction 3 checkpoints register A prior to instruction 8 storing to register A.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

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